REMARKS

Reconsideration and allowance of the subject patent application are respectfully requested.

Claims 21-25 and 33 were objected to on the basis of certain informalities. Claims 21 and 33 have been amended as kindly suggested by the Examiner. The remaining claims 22-25 are now canceled and thus the objections to these claims are moot.

Claims 2 and 18 were rejected under 35 U.S.C. 112, second paragraph, as allegedly being indefinite. To overcome this rejection, claim 2 has been amended to refer to refer to the first and second unit circuits. Claim 18 is canceled and thus the rejection of this claim is moot.

Claims 3 and 29-33 were rejected under 35 U.S.C. Section 112, first paragraph, as allegedly being based on subject matter not described in the specification. Claim 3 is canceled and thus this rejection with respect to this claim is moot. Applicant respectfully traverses this rejection with respect to claims 29-33.

Claim 29 recites:

> the first circuit is (i) a processing circuit which uses output of one of the first unit circuits, (ii) a second unit circuit for a second shift register different from the first shift register, and (iii) a processing circuit which uses output of the second unit circuit of the second shift register.

Claims 30-33 contain the same description of the first circuit. The office action maintains that the original disclosure does not provide support for this language.

Applicant respectfully traverse this contention because the recitation regarding the first circuit of claims 29-33 is in fact fully supported by the original disclosure.

For example, Figure 14 shows by way of example and without limitation a first circuit (which is shown as being disposed in the physical space between a first unit circuit of a preceding output stage (**e.g., F/F1(1)**) and a first unit circuit of a following output stage (e.g., **F/F1(2)**) which is made up of:

(i) a processing circuit (e.g., **WR1(1)**) which uses output of one of the first unit circuits (e.g., **F/F1(1)**);

(ii) a second unit circuit (e.g., **F/F2(1)**) for a second shift register different from the first shift register; and

(iii) a processing circuit (e.g., **WR2(1)**) which uses output of the second unit circuit (e.g., **F/F2(1)**) of the second shift register.

Consequently, the claimed subject matter is fully and completely supported by the original disclosure and withdrawal of the Section 112, first paragraph, rejection of claims 29-33 is respectfully requested.

The Advisory Action indicates that claim 29 requires "the first circuit is a processing circuit which uses output of ... a processing circuit which uses output of the second unit circuit of the second shift register." However, Applicant respectfully submits that this interpretation is based on a misreading of claim 29. For clarification, claims 29-33 have been amended to recite that the first circuit is (i) a processing circuit which uses

output of one of the first unit circuits, (ii) a second unit circuit for a second shift register different from the first shift register, and (iii) a processing circuit which uses output of the second unit circuit of the second shift register. As explained above, such a first circuit is shown by way of example and without limitation in Figure 14.

Claims 1, 2, 8-10, 13-18, 20-25 and 29-33 were rejected under 35 U.S.C. Section 102(b) as allegedly being "anticipated" by Kihara et al. (U.S. Patent No. 5,889,504).

Applicant respectfully traverses this rejection.

Each of independent claims 29-33 recites that *signal paths for the first and second shift registers are provided separately for each of the first and second shift registers on respective sides of a circuit alignment of the first and second unit circuits of the first and second shift registers*. As described in the subject patent application with reference to the example embodiments, this arrangement of signal paths has various advantages. See, e.g., pages 50-51 of the subject patent application.

Figures 5A, 5B and 6 of Kihara et al. and the accompanying description in cols. 7 and 8 do not show or suggest providing signal paths for different shift registers separately on respective sides of the circuit alignment. Notwithstanding the annotations shown on page 8 of the office action, Figure 6 clearly shows that the signal paths for each of the various shift register portions SR1, SR2, SR3 and SR4 of block 11 are provided on both sides of the portions. (Although not expressly shown in Figure 6, Kihara et al. teaches that the signal paths for the shift register portions of blocks 12, 13 and 14 are arranged in

the same way as for block 11. In this regard, see col. 7, lines 35-37 which mentions the unillustrated connections for these blocks.) There is no teaching or suggestion of providing signal paths for first and second shift registers separately on respective sides of the circuit alignment as claimed. Because Kihara et al. does not disclose the claimed signal path arrangement, Kihara et al. cannot anticipate claims 29-33 or the claims which depend therefrom.

Claims 1-3, 8-10, 12-18, 20-25 and 29-33 were rejected under 35 U.S.C. Section 102(e) as allegedly being "anticipated" by Azami (U.S. Patent No. 6,702,407).

Applicant respectfully traverses this rejection.

Regarding Azami, the office action asserts (see, e.g., first full paragraph on page 16 of the office action) that the first four flip-flop circuits FF in Figure 3 are the first shift register and the "next" (unshown) four flip-flop circuits are the second shift register. However, Applicant respectfully submits that all of these flip-flips are quite clearly part of the same shift register.

In addition, independent claims 29-33 each requires that a second unit circuit for the second shift register be part of a first circuit disposed in the physical space between first unit circuits of the first shift register. The nominal first and second shift registers identified in the office action are not arranged in this manner. Specifically, the first four flip-flops (the nominal first shift register) and the second four flip-flops (the nominal

second shift register) are not arranged so that a second unit circuit of the second shift register is disposed between first unit circuits of the first shift register, as claimed.

Moreover, even under the office action's erroneous view of Azami, the signal paths for the allegedly "different" shift registers are not provided separately on respective sides of the circuit alignment. Specifically, signal paths for the first four flip-flops FF in Figure 3 of Azami are clearly shown as being provided on both sides of the circuit alignment. Indeed, the signal lines pointed to by the annotations shown on page 14 of the office confirm this. There is no disclosure or suggestion in Azami of providing the signal paths for the first four flip-flops FF on one side of the circuit alignment and the signal paths for the next four flip-flops on the other side of the circuit alignment.

At least because of these deficiencies, Azami cannot anticipate claims 29-33 or the claims that depend therefrom.

Claims 1-3, 8-10, 13-18, 20-25 and 29-33 were rejected under 35 U.S.C. Section 102(e) as allegedly being "anticipated" by Washio et al. (U.S. Patent No. 6,724,361).

Applicant respectfully traverses this rejection.

Regarding Washio, the office action asserts (see, e.g., last two lines on page 17 of the office action and continuing onto page 18) that the first four flip-flops 23 in Figure 11 are the first shift register and the next four flip-flops 23 are the second shift register. Here again, Applicant submits that all of these flip-flops are part of the same shift register.

In addition, as with Azami, Washio does not disclose or suggest that a unit circuit for the nominal second shift register is part of a first circuit disposed in the physical space between unit circuits for the nominal first shift register.

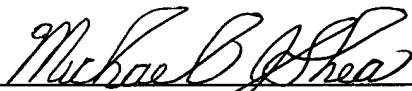
Moreover, even under the office action's erroneous view of Washio, the signal paths for these allegedly "different" shift registers are not provided separately on respective sides of the circuit alignment. Specifically, signal paths for the flip-flops FF in Figure 11 of Washio are provided on both sides of the circuit alignment and the annotations shown on page 19 of the office action confirm that signals lines for any given flip-flop are disposed on both sides of that flip-flip. There is no disclosure or suggestion in Washio of providing the signal paths for the first four flip-flops on one side of the circuit alignment and the signal paths for the next four flip-flops on the other side of the circuit alignment. Because of these deficiencies, Washio cannot anticipate claims 29-33 or the claims that depend therefrom.

Claim 11 was rejected under 35 U.S.C. Section 103(a) as allegedly being made "obvious" by Azami. Even assuming the image data in Azami is modified to be analog image data, Azami is still defective with respect to claim 31 (from which claim 11 depends) as discussed above. Consequently, claim 11 patentably distinguishes over Azami.

The pending claims are believed to be allowable and favorable office action is respectfully requested. Should the Examiner feel that further discussion would facilitate allowance of this application, the Examiner is encouraged to contact the undersigned.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: 

Michael J. Shea
Reg. No. 34,725

MJS:mjs

901 North Glebe Road, 11th Floor
Arlington, VA 22203-1808
Telephone: (703) 816-4000
Facsimile: (703) 816-4100